Hardware Description Language (HDL) Parser

AI Studienprojekt SS 2020

Dr.-Ing. Pascal Sasdrich
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The Project

A Hardware Description Language (HDL) Parser
Motivation and Background

GOAL:
- development of secure hardware
- protected against physical attacks

METHODOLOGY:
- hardware + security in HDL (e.g., Verilog)
- translation into gate-level netlist (HDL)
- synthesis uses existing tools

PROBLEM:
- synthesizer optimized for area, speed or power but **NOT** security
- synthesis tools can even destroy security!

SOLUTION APPROACH:
- parse gate-level netlist (given as HDL)
- formal verification of gate-level netlist (for security)
Hardware Description Language (HDL) Parser

Tasks and Goals

Front-End Processing (Abstract Syntax Tree generation)

Task 1: *Lexical Analysis of gate-level netlist in Verilog (HDL)*

Task 2: *Syntax Analysis of gate-level netlist in Verilog (HDL)*

Task 3: *Semantic Analysis gate-level netlist in of Verilog (HDL)*

Back-End Processing (Translation into Intermediate Format)

Task 4: *Translation of AST into Intermediate Format for further processing*

Extensions:

Extension 1: *Support for additional HDLs (e.g., SystemVerilog and VHDL)*

Extension 2: *Support for different intermediate formats (i.e., additional back-end modules)*

Extension 3: *Analysis of intermediate formats for security and implementation properties*
Hardware Description Language (HDL) Parser

Schedule and Timeline

**Start:** April 6, 2020  
**End:** June 12, 2020  
**Duration:** 10 weeks  

**Organisation:**
- Kick-off meeting Week 1 (April 6 - April 10)  
- Status meetings Week 3, 5, 7 and 9  
- Final meeting Week 10 (June 8 – June 12)
Project Summary
Requirements and organisation at a glance
## Hardware Description Language (HDL) Parser

### Project Summary

<table>
<thead>
<tr>
<th>Task:</th>
<th>Implementation of a Hardware Description Language Parser</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timeline:</td>
<td>April 6, 2020 – June 12, 2020 (10 weeks)</td>
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<tr>
<td>Number of students:</td>
<td>1 (min) / 3 (max)</td>
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<tr>
<td>Target group:</td>
<td>Bachelor students</td>
</tr>
<tr>
<td>Prerequisites (mandatory):</td>
<td>Informatik (I/II), Programmieren in C</td>
</tr>
<tr>
<td>Prerequisites (optional):</td>
<td>Software-Engineering, Datenstrukturen</td>
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<tr>
<td>Application documents:</td>
<td>Current Transcript of Records</td>
</tr>
<tr>
<td>Contact person:</td>
<td>Dr.-Ing. Pascal Sasdrich (<a href="mailto:pascal.sasdrich@rub.de">pascal.sasdrich@rub.de</a>)</td>
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Thank you!

Questions?

Dr.-Ing. Pascal Sasdrich

pascal.sasdrich @rub.de