Fast Circuit Evaluation in the Presence of Faults

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Boolean Circuit

- Combinational Logic

- Sequential Logic

https://cdn.sparkfun.com/assets/learn_tutorials/2/1/6/20-combinational_circuit.png
Normal Evaluation:

Fault Injection:

- Idea: Generate Report:
  
  „100% of one-bit faults can be detected.
  5% of two bit-fault can be detected.“
Your task

- Parse a netlist into a graph representation
- Evaluate the netlist given an input and a set of faults
- Generate a report about detectable faults
- (Optional: Pinpoint why a fault was not detected)
Requirements / Benefits

• Who are you?
  – 2 – 3 Students
  – Bachelor’s or Master’s level

• What do you have to know?
  – Some level of C / C++ knowledge

• What are you going to learn?
  – Representations of hardware circuits
  – Circuit Simulation
  – Concepts of Fault Injection

• Follow-up perks?
  – SHK/WHB Jobs are available
Organization

• Start: First Week of April
• End: Mid July

• Bi-weekly meetings

• Goal: Simulate one-bit faults in any sequential circuit

• Extended Goals:
  » Pinpoint the cause of non-detection
  » Evaluate multiple-bit faults
  » Support multiple netlist formats
Contact

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